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# dsp valley newsletter 3

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**designing smart products**







## ICsense (BE) and TheraSolve (BE) cooperate on electronic patch development

Forgetfulness to take medicines is the most frequently cited reason (64% of the cases) for noncompliance and today's reminder methods are complex and impact on patient's lives significantly. The novel electronic patch from TheraSolve (which looks like a nicotine patch), brings an innovative solution to the problem by applying a controlled mild stimulus to the patient as a reminder to take its medicine.

For reasons of size, cost, reliability and discretion, the number of components is minimized to a battery, a custom ASIC and a few essential passive components.

ICsense
THE IC DESIGN COMPANY

**continuation on page 2**

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## Keeping track of time

The patch needs to operate for one entire week while delivering high-voltage, low energy reminder 'pulses' to the patient and accurately keeping track of time without expensive and bulky crystal-based timing generators. To accomplish this, a custom IC with accurate on-chip oscillator

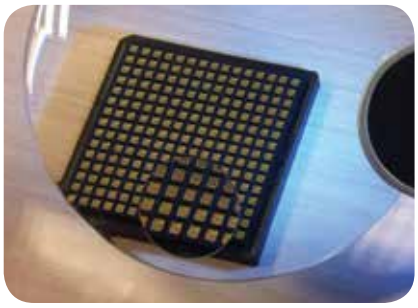

***Pharmaceutical therapy bundled with TheraSolve adherence technology***

(1000ppm) was developed by ICsense. In developing the solution, TheraSolve performed a range of elaborate user studies in recent years to determine the right voltage, pulse shape and timing for the optimal 'digital touch' reminder. The pulse characteristics are fully programmable on chip and can be tailored in future to target patient profiles.

Drawing sufficient voltage and power from a single, high-resistance button cell battery, many times during a single week's use has been a challenging system level design issue to solve. ICsense tackled the problem using state-of-the-art DC/DC converter techniques combined with clever duty cycling of the power generation system. The complete solution was achieved with the least amount of external components. To ensure maximum patient comfort, the total thickness of the patch is restricted by the battery dimension alone and is less than 2mm.

## Pharmaceutical Applications

The use of the patch is made as simple as possible. Just apply the self-adhesive patch to the skin 'Stick and Play'. Once it is in place, the patch is ready to do its job, operation starts automatically when applied to the skin thanks to an innovative proximity detection system. MemoPatch® can be fully preprogrammed during production with the right medication intake



***The tiny electronic heart of the MemoPatch® under the magnifying glass***

schedule uploaded to it. With this product, TheraSolve is positioning itself as a genuine medication adherence innovator and could play a key role in enhancing medical outcomes in the areas of Parkinson's disease, Alzheimer's disease, multiple sclerosis, HIV, hepatitis C, oncology, epilepsy, post-transplantation, diabetes and many others.

## From Design to Market

The technology at the heart of this unique medical wearable has been developed with the financial support of the Flemish Institute of Science and Technology (IWT). MemoPatch® is now beyond the prototyping phase and is currently being validated in several sci-

Preface

# Smart Cities: hype or reality?

**Last year around this time, the Preface of the Newsletter drew your attention to the fact that DSP Valley is partner in a European "Regions of Knowledge" project focusing on Embedded Systems for Smart Cities (CLINES). Our main cluster partners in this project are from Spain (GAIA), Denmark (BrainsBusiness) and Germany (BICCnet). The overall objective of the project is to drive economic development in the field of Embedded Systems for Smart Cities, through regional and joint actions. So, where are we today with the CLINES project?**

From the typical six dimensions of a Smart City (Smart Living, Smart Environment, Smart Mobility, Smart Governance, Smart Economy and Smart People), we have decided to focus on the first three, as our initial analysis showed that they are best represented in the combined regions. As a subtopic of Smart Environment, the matter of Smart Energy is an important dimension to be taken into account as well.

Within this focus, we have performed a SWOT analysis of the four regions to look for complementarities in the combined ecosystems. We reported on this work for the first time in an innovation workshop in June 2014 in Brussels, where companies from the partner regions also presented their solutions for Smart Cities (Siemens DE, Nexmachina ES, Seluxit DK). Right now, we are working on a Joint Action Plan to build a vibrant European ecosystem around Embedded Systems for Smart Cities. We intend to run this Joint Action Plan by you in the coming months through local or international workshops, so that we can incorporate your feedback on our ideas.

In general, we have built a solid 4-way relationship among the project partners while working on the planned activities of the project, and we have found a common ground for a cross-cluster approach to Smart City challenges. The close cooperation with clusters from Spain, Denmark and Germany has also helped in finding partners for European projects (for instance on smart crime fighting). As such, we have laid the foundations for a further extension of the partnership to include other European clusters and regions (France, UK) and to explore Smart City opportunities beyond the European borders as part of our internationalization strategy (US, Asia, Latin America – continents where today's mega-cities can be found).

Of course, you are still wondering what the answer is to the question above this

entific studies. TheraSolve has already secured the interest of major international pharmaceutical companies for innovative applications of the patch. Concurrently, volume production processes are being fine-tuned to allow for high-yield, large volume manufacturing of the device. The company is now investigating additional applications for its patch technology that will emerge through synergies with other technologies in future including those lying at the convergence between wireless and internet of things functionalities. ■

***Discrete MemoPatch® medical therapy adherence technology in use***

Preface: are Smart Cities for real, or are they just another hype, along with other "Cyber-Physical Systems"? Although an in-depth answer to this question would lead us too far, one or two remarks can definitely be made. First, progressing urbanization is a worldwide trend that cannot be ignored: by 2040, over 65% of the world population will live in urban areas. So, yes, maybe one day "mayors will rule the world" (see Barber 2013). At the same time, Smart Cities are more of a vision of the future than a reality today. There are many scattered initiatives (both top-down and bottom-up) to harness the power of (embedded) technology for the benefit of the citizens, but there is a lack of a coherent long-term approach bringing all stakeholders together in a common vision and a united effort. With our CLINES project, we are trying to help build that approach on a European and global scale.

**continuation on page 5**

# MathWorks Expands Support for Xilinx Zynq-7000 All Programmable SoCs and Altera SoC FPGAs

## Time-to-production for programmable SoC FPGAs is reduced using Model-Based Design

MathWorks has announced its expanded support for targeting Altera® SoC FPGAs and Xilinx® Zynq®-7000 All Programmable SoCs. The newest release of MATLAB and Simulink allows engineers and scientists using Model-Based Design to reduce their time-to-production with a higher degree of confidence, all within a single tool environment.

Devices in the Xilinx Zynq-7000 family and the Altera SoC family incorporate a dual-core ARM® Cortex®-A9 coupled with powerful programmable logic fabric. This combination enables engineers and scientists to design and implement algorithms on a single chip that consumes less space and power. Now, MathWorks provides a guided workflow to develop and simulate algorithms which can be validated quickly and deployed onto these SoC devices, leveraging automatically generated C and HDL code.

In addition to existing support for the Xilinx ISE® Design Suite and the Zynq Intelligent Drives Kit, the extended support provides integration with the Xilinx Vivado® Design Suite, Zynq SDR development platforms, and Altera SoCs. As a result engineers and scientists can prototype quickly on a hardware platform and then incorporate the generated C and HDL code into production environments through the use of Altera and Xilinx tool sets.

*"MathWorks expects semiconductor vendors to continue to expand their offerings of heterogeneous, programmable SoCs"* said Amnon Gai, manager, corporate development and partner programs at MathWorks. *"As applications are migrating from processor-only technology to programmable SoCs, the ability to generate C and HDL code from MATLAB and Simulink makes MathWorks uniquely positioned to address the growing demand for a unified hardware/software workflow using Model-Based Design."*

The expanded support for Xilinx Zynq-7000 All Programmable SoCs and Altera SoC FPGAs is currently available in Release 2014b. MathWorks also offers a two-day training class to help engineers get up and running quickly on this technology. ■

### About Mathworks

MathWorks is the leading developer of mathematical computing software. MATLAB®, the language of technical computing, is a programming environment for algorithm development, data analysis, visualization, and numeric computation. Simulink® is a graphical environment for simulation and Model-Based Design of multidomain dynamic and embedded systems. Engineers and scientists worldwide rely on these product families to accelerate the pace of discovery, innovation, and development in automotive, aerospace, electronics, financial services, biotech-pharmaceutical, and other industries. MathWorks products are also fundamental teaching and research tools in the world's universities and learning institutions. MathWorks was founded in 1984 and has more than 3,000 employees in 15 countries. Our headquarters is located in Natick, Massachusetts, United States. MathWorks' Benelux office is located in Eindhoven.

# New Synopsys ASIP Designer Tool Speeds Development of Application-Specific Instruction-Set Processors by 5X

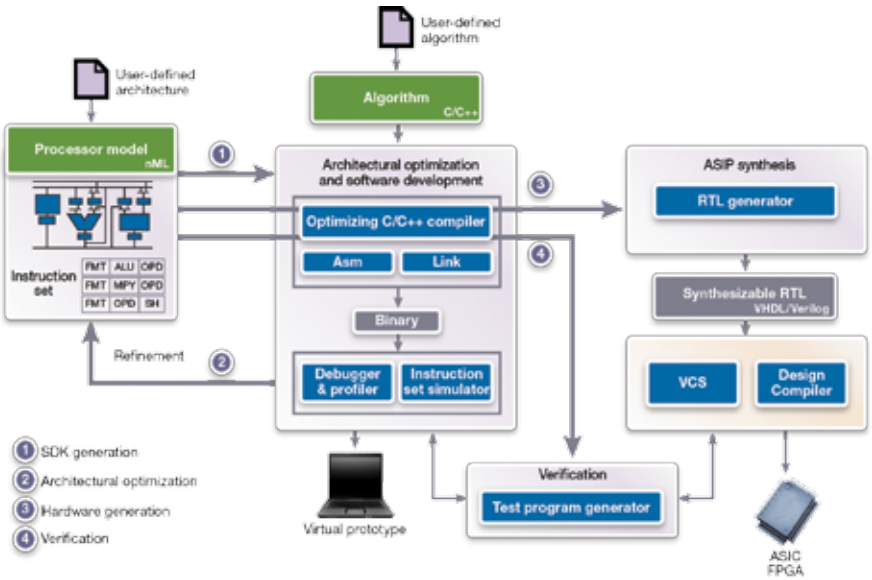
SYNOPSYS®
Accelerating Innovation

**Automatic Generation of the Software Development Kit in Parallel with the Hardware Model Enables Rapid Architectural Exploration to Optimize ASIPs for Power, Performance and Area**

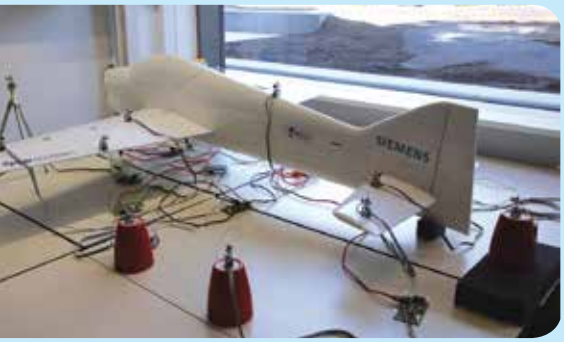
### Highlights:

- Synopsys' ASIP Designer automates the design of application-specific instruction-set processors and programmable accelerators
- Leverages Synopsys' proven ASIP tool technology that has been used by more than 50 companies to design hundreds of successful products
- Unique "compiler-in-the-loop" feature enables use of application code to optimize ASIP architecture for performance and power
- Integrated LLVM-based compiler front-end and OpenCL kernel language support enables efficient compilation of C, C++ and OpenCL-based application code

Synopsys, Inc. (Nasdaq:SNPS) has announced availability of its new ASIP Designer tool that speeds the design of application-specific instruction-set processors (ASIPs) and programmable accelerators. ASIP Designer's language-based approach allows the automatic generation of synthesizable RTL and software development kits (SDKs) from a single input specification, accelerating the processor design and verification effort by up to 5X compared to traditional




# AnSem - Automatic localization system reduces substantially testing time for vibrational analysis of large mechanical structures



Vibrational analysis and testing is a critical phase during the design and development of mechanical structures like bridges, planes and cars. Siemens Industry Software NV offers vibration testing solutions where up to a thousand accelerometers can be placed on these structures. An essential factor in the interpretation of the test results is the exact positioning of the accelerometers on the structure, i.e. determining the 3D position coordinates of each sensor. Currently the localization measurement is performed with expensive optical equipment or manually and can take up to a week for larger structures such as airplanes.

AnSem, Siemens Industry Software and the other partners in the IWT-SBO project 'OmniTrack' developed an automatic localization system that dramatically reduces the testing time as one of the project's use cases.

The basic idea of this so-called "dense mesh" localization system is that all nodes measure the distances to their neighbors. This information is used to calculate the 3D position of all sensors. AnSem developed the hardware, software and algorithms for the intelligent mesh nodes, Siemens Industry Software designed the 3D localization software.

A study of indoor localization techniques in the framework of this project showed that the ultrasound measurement principle is the best candidate for indoor localization in these dense meshes. Ultrasound detection is a technology that is widely used: it combines

manual approaches. ASIPs are deployed in a wide range of signal-processing intensive applications, including wireless base stations, mobile handsets, audio processing, image processing and cloud computing.

*"Using Synopsys' ASIP tools we've developed and deployed a full line of highly differentiated AudioSmart products. These products are based on the Conexant Audio Processing Engine, or CAPE, a Conexant-designed DSP,"* said Saleel Awsare, vice president and general manager at Conexant. *"Application-specific architecture optimizations make CAPE highly efficient for far-field voice and audio playback processing, and Synopsys' tools assure ease of creation and programmability. By continuing to invest in ASIP tool technology, Synopsys is helping Conexant create market-leading domain-specific products."*

ASIP Designer enables users to explore multiple processor architecture alternatives in minutes. Using a single input specification in the nML language, the tool automatically generates both the synthesizable RTL of the processor as well as an SDK that includes an optimizing C/C++ compiler, instruction set simulator, linker, assembler, software debugger and profiler. This ensures consistency of the hardware and the SDK at all stages of the design process. The patented compiler generation technology includes an LLVM compiler front-end and support for the OpenCL kernel language. Immediate availability of the compiler enables users to run their C, C++ and OpenCL application code on the automatically-generated instruction-set simulator as soon as the nML-based description is available. With this unique "compiler-in the-loop" approach as well as the extensive profiling capabilities of the debugger, ASIP Designer users can rapidly analyze and explore ASIP architectures and instruction sets to find the optimal power and performance design points for the target application.

ASIP Designer also automatically generates a SystemC-based transaction-level model, allowing pre-silicon software development using virtual prototypes such as those designed with Synopsys' Virtualizer™ tool set. A common and easy-to-use flow from RTL generation to instantiation in the HAPS® FPGA-based prototyping system, in addition to the automatic generation of JTAG-based on-chip debug logic, enables designers to integrate the ASIP into the system-on-chip (SoC) design and connect the prototype with real-world I/Os to validate the hardware-software integration.

A wide range of example ASIP designs for highly differentiated architectures, provided in nML source code, allows designers to quickly start designing their own ASIP that targets their specific application requirements.

*"ASIPs offer distinct advantages over standard DSPs and fixed hardware in many data plane and signal processing applications,"* said John Koeter, vice president of marketing for IP and prototyping at Synopsys. *"Synopsys' new ASIP Designer tool, built on proven technology used in hundreds of products in the market, helps design teams speed the development of custom processors and programmable accelerators tuned to their specific application. ASIP Designer gives users the ability to explore and optimize processor architectures for the best power, performance and area, giving them a distinct advantage in creating highly differentiated products."* ■

low cost and simple synchronization with good accuracy.

In the OmniTrack sensor network built by AnSem, each node is equipped with an ultrasound transceiver and an MCU. This node calculates the distance between its neighboring nodes. The transceiver nodes are mounted on mini motors that rotate the transceiver to cover the complete space above the nodes base. The developed algorithm is robust and compact enough to be performed by the basic MCUs on the nodes and to obtain the required cm accuracy.

A central hub transmits the synchronization signals and collects the distance data from the nodes. A central computer equipped with the Siemens 3D localization software reconstructs off-line the 3D locations of the sensors on the structure using a "Dense Mesh Localization Algorithm". To obtain the required cm accuracy, redundancy in the mesh is used. The nodes are localized node per node, based on as many measurements as possible, including newly-localized nodes.

These results were presented on a public workshop, with more than 60 interested attendees, held at ESAT on April 3rd. The consortium of research partners consisted of KULeuven ESAT-MICAS, Flanders Make, Siemens Industry Software and AnSem. ■

SIEMENS

AnSem
Innovation on chip

**continuation from page 3**

## Preface

The partners in the CLINES project however are mainly bringing together solution providers (technologies and applications). But to find the real use cases, we have to reach out to the cities. Therefore, we are looking forward to establish more intensive contacts with cities in our target regions. Finally, this will result in a quadruple or even quintuple helix: industry, academia, local authorities, finance and the users. It is clear that in this context, cities have a double role, both as local authority and as voice of the user. We can't wait hearing from the cities, what they are looking for to become SMART!

Best regards,
Peter Simkens
Managing Director

# SmartNodes' technology in a nutshell

SmartNodes

SmartNodes proposes a new way to illuminate public spaces: "Light where and when needed". In contrast with a classic 'always on' lighting or even with a reduced lighting during the off-peak hours (independent of the traffic), SmartNodes wants to innovate by offering an on demand lighting: only when and where road users (car, bike, pedestrian, etc.) are present.

SmartNodes Smart Lighting system (SLS) control modules create "light bubbles" following the road users wherever they go. By dynamically varying the light emitted by each luminaire, each road user type receives a dedicated light bubble especially adapted to his needs and his speed. Maximal energy savings (up to 80%) are achieved while maintaining the same quality of light and the same level of security as the usual static power level.

The proposed technology is innovating at several levels and overcomes many limitations of competitive solutions. By providing a decentralized solution and an autonomous decision at the luminaire level, it avoids the communication bottlenecks of a centralized system and maximizes the robustness of the system. Each SLS module communicates with its nearest neighbors and decides alone what to do. A failure in one part of the network remains local and does not impact the functioning of the whole network. Moreover, the network of these modules is easily extensible.

To support "Smart Cities" development, an optional access point can be added to the network of these SLS modules to allow remote monitoring and remote access of information like, but not limited to, luminaires status, power consumption statistics, traffic statistics, sensors status, etc. Additional sensors can be plugged into the street light network. Remote control of the network to reconfigure it or to switch from dynamic to static operation is also possible.

## Smart Street Lighting in Wavre

SmartNodes solution was already implemented in numerous industrial parks or

car-pooling parkings. It is now deployed in Wavre in a residential area: the largest intelligent public street lighting in Belgium. This huge project is composed of three different phases: about 300 modules at the "Village Expo" (Limal), at the "Lotissement des Vents" (Wavre) and in the "Ruelle du Coulant d'Eau" (Wavre). These lighting street poles are equipped with the autonomous SmartNodes module (SLS-R2-A) completed to iGuzzini Luminaires.

The project is part of a futuristic vision of a Smart City based on its public lighting network widely deployed on its territory. By combining dynamic management of this lighting with use of the lighting network to convey some information, the project is linked to different thematic "Smart Cities":

- Economy: energy performance of the solution without sacrificing the comfort and safety of users but all of this infrastructure contributes to the collection and sharing of data necessary for the control of the city. The solution allows to adapt the resources closer to the needs and better control and budgets;
- Environment: reduction of CO2 emissions and reduction of light pollution;
- Mobility: traffic management through better adapted to traffic statistics gathered, preventive signaling based traffic and faster response in case of need;
- Governance: resource management and use of information and communications technology (ICT);
- Human capital: a mobile user and interactive relationship without sacrificing visual comfort and safety;
- Housing: a better balance between the need for urban lighting and the respect of a nightlife of biodiversity but also the need for harmony and aesthetics of lighting in the urban landscape.

The project of the City of Wavre was also inspired by the objectives of the European Commission described in its June 2013 "Lighting the cities – Accelerating the deployment of innovative lighting in European cities".

The participatory nature of the project is planned after the renovation phase of the lighting in the residential area of the Expo Village:

- Technology is configurable (level and duration of illumination, etc.). It will be proposed citizen marches and roundtables to assess, validate or modify these settings. It will be essential to unite the population of these neighborhoods or street in this new type of intelligent lighting.
- The technology is scalable. An exchange of views will also be offered to a group of residents to explain the new services related to smart lighting, uses and interests for the community but also for the inhabitants themselves.

In summary, a participating nature project, not around a concept, but a practical and experimental realization. Demonstrations of new intelligent and interconnected lighting technology is required to demonstrate explicitly the potential benefits which benefit the city of Wavre by enrolling in the concept of the Smart City.

The Régie d'Electricité de Wavre ("REW") commissioned by the City of Wavre took few months to learn about available technologies, to understand, to prepare specifications and to launch a tender. After contract award, the various stakeholders, namely the integrator (CDEL), the installer (CofelyFabricom-GDF Suez), the pole supplier (Alp-belgium), the luminaires provider (Iguzzini) and the provider of the intelligent modules (Smartnodes) were associated by REW at several preparatory meetings to coordinate the work.

All the preparatory work took a year and began in late 2013. The project now is in its implementation. The start took place in early December 2014 and should be completed by June 2015. A first test on part of the site was demonstrated in April 2015 in presence of Belgian Prime Minister Charles Michel. A first impact assessment is planned in the course of 2015 and will be monitored by the REW but also by the different project stakeholders. ■

# Barco Silex Partners with Rambus to Combat Security Threats in Point-of-Sale Market

## Enabling expansion of DPA Countermeasure solutions beyond traditional smartcard market

BarcoSilex

Rambus Inc. (NASDAQ:RMBS) has announced that its Cryptography Research Division has entered into a partnership agreement with Barco Silex. Through this agreement, Barco Silex can develop DPA-resistant solutions that help accelerate time-to-market of security-based products. Barco Silex will utilize Cryptography Research differential power analysis, or DPA, countermeasure technology to help protect against security risks in a variety of point-of-sale applications, including banking, retailing, mass transit, and wireless telecommunications.

*"Side-channel attacks are becoming more prevalent, and we need a sound solution to combat this growing risk to ensure customer confidence and protect high value assets,"* said Sébastien Rabou, Product Manager at Barco Silex. *"The partnership with Rambus allows us to have access to the world-class cryptography engineers while developing solutions to benefit the point-of-sale market."*

*"The risk of security breaches continues to explode and customers need to quickly get secure solutions into the market",* said Dr. Simon Blake-Wilson, vice president of Products and Marketing of the Rambus Cryptography Research division. *"By partnering with Barco Silex, we have created another channel that will accelerate time-to-market with advanced security technology."*

Concerns about DPA security attacks originated in the smartcard market; however, the potential for these attacks is spreading into many other markets. For this reason, there is a need for DPA countermeasures to be adopted across all markets where valuable financial and personal data is being handled. Today, products commonly at risk include point-of-sale devices, mobile phones, secure USB flash drives, pay television set-top boxes, and optical disc players among others.

DPA is a type of side-channel attack that involves monitoring variations in the electrical power consumption or EM emissions from a target device. These measurements can then be used to derive cryptographic keys and other sensitive information from chips. Rambus Cryptography Research DPA countermeasure technologies are a proven solution for protecting devices against the extraction of cryptographic keys and private data through side-channel attacks. Highly flexible, these solutions can be optimized for performance, size and security level, allowing customers to help fend off unauthorized access to critical information. Having discovered side-channel attacks, Cryptography Research scientists have developed a comprehensive portfolio of application-specific hardware core and software library solutions that chipmakers can use to build DPA resistant products. These DPA resistant solutions can be integrated into a wide range of SoCs, including power-sensitive mobile applications, highly secure anti-tampering and performance-driven multi-core processors.

Barco Silex has joined the Rambus Partner Program, which will enable further collaboration on other combined IP blocks offerings between the two companies. ■

# Trinean wins cheque of 25.000 euro for quality improvement of microfluidic plastic disposables –Test & Measurement Solutions

**Ghent-based life sciences company Trinean has won the 'Time for a Boost' innovation contest 2015, an initiative of Test & Measurement Solutions, earning a much-coveted €25,000 check in the process.**

The professional jury was impressed with the company's suggestion to implement an automated optical inspection solution in the coating process of microfluidic plastic disposables.


***From left to right: Kurt Hensen (CEO Test & Measurement Solutions) – Kris Naessens (Head of production, Trinean NV) - Philippe Stas (CEO Trinean NV)***

Trinean is a Belgium based instrumentation company, bringing micro-volume molecular spectroscopy to the next level by combining best in class analytical software with a highly standardized read-out platform. Founded in 2006 as a spin-out of the Ghent University, Belgium and Imec Leuven, Belgium, the company commercializes two instruments, the XposeTM for 'Touch & Go' biomolecule quantification and the DropSense96TM, analyzing up to 96 samples, using microfluidic chips for standardized sample analysis (DropPlates and Xpose Slides). The Trinean platform is complemented with a software toolbox for improved data interpretation and lab-automation.

DNA, RNA or protein tests are very expensive and the required samples (blood, tumor, tissue, …) are very scarce. This is why it is important that any biological sample is used efficiently with every test.

To be sure that every sample contains enough DNA,RNA or proteins Trinean developed plastic disposables, on which 16 samples can be dosed in combination with lab equipment to do an effective measurement. As a very small drop of fluid (2 µl) is used for this measurement each disposable is made hydrophilic by a specific coating technology. This way each sample can be absorbed automatically in very small canals and can protected against vaporization.

A severe optical inspection of the hydrophilic coating process is the only way to guarantee the quality of the plastic disposables. This is why Trinean will work together with Test & Measurement Solutions to implement an automated vision inspection solution. It will save time and money by avoiding unnecessary DNA, RNA or protein tests.

Kurt Hensen, CEO of Test & Measurement Solutions: *"The three nominees each had a very strong proposal to improve the quality of their products. The professional jury was impressed by the suggestion of Trinean to implement an automated vision inspection system. This customized solution will be a great added value for the scalability of Trinian's activities. In addition it will greatly improve their precision, traceability and process control of their coating process."*

This was confirmed by Philippe Stas, CEO of Trinean: *"The quality of our optical lab instruments and associated microfluidic disposables are of particular importance to Trinean, whose portfolio is worldwide consulted in diagnostic centers and biobanks for sample analysis"*. Kris Naessens , head of production explains: *"This check helps our organization with the development of an automated vision inspection system for the microfluidic disposables. This system will ensure constant quality with traceability per lot or article and therefore, answers the needs of all customers who operate in a regulated environment."*

Trinean follows ViskoTeepak and Cochlear, our winners of 2013 and 2012. Other Belgian nominees this year were Amcor Flexibles (Halen) and Canberra Semiconductor (Olen). Congratulations to all of them! Discover their stories on www.timeforaboost.be.

Time for a Boost is a yearly cooperation in Flanders, Belgium with Innovatiecentrum Vlaanderen, BAN Vlaanderen, Agoria, JCI and DSP Valley. ■

TEST & MEASUREMENT SOLUTIONS

trinean

# Imec Reports 9 Percent Growth in 2014

Imec's revenue for the fiscal year ended December 31, 2014 totaled 363 million euros, a 9 percent growth from the previous year. The fiscal year end total includes the revenue generated through R&D contracts from international partners, collaborations with universities worldwide and funds from European research initiatives. The annual revenue figure also covers a yearly grant from the Flemish government totaling 48.8 million euro in 2014, and a 4.1 million euro grant from the Dutch government to support the Holst Centre, a research center setup by imec and TNO.

In 2014, imec filed a record number of patents (143), achieved notable industry awards and published prominent scientific papers (950). Our talent pool grew to a total of 2,188 employees by the end of 2014.

Two new spin-offs were launched in 2014 - Luceda Photonics, active in photonics design, and Bloom Technologies, focusing on wearable health monitoring for expectant mothers. Moreover, imec opened a new office building, as it aims to expand further across its R&D focuses. Additionally, the center started building a new cleanroom that adheres to the very latest standards with a significant footprint for the most advanced semiconductor tools. The new cleanroom will enable the organization to remain at the forefront of nanoelectronics research and development, offering a neutral platform where all the key players from the semiconductor value chain closely collaborate to advance the next generation technology nodes and advancing industrial innovation.

Imec IC-link, offering SMEs, universities and research institutes access to advanced foundry technologies, assembly, test, and place and route services

has a customer base of more than 300 SMEs and 700 universities and research institutes (through Europractice service), IC-link tapes-out an average of 500 designs per year. ■

# TICO Lightweight Compression, Winner of the "IABM Game Changer Awards 2015"

"intoPIX TICO Lightweight compression for Live 4K over IP" is the Winner in the Content and Communication Infrastructure category for the IABM Game Changer Awards 2015 at NAB 2015.

NAB Show vendors devote significant time and resources to bringing their best new developments to the show floor. The IABM Game Changer Awards honor this effort and the forward-looking solutions it yields. The judging panel has identified intoPIX TICO compression technology as one of the leading products to be exhibited at NAB Show 2015, Las Vegas.

TICO is a the new disruptive lightweight compression technology developed by intoPIX, which enables 4K/UHD to be transported over legacy SDI infrastructure and 10GbE networks with the smallest latency, the smallest complexity and a preserved high quality. The technology is currently being pushed at the SMPTE as an RDD.

**Main characteristics of TICO are:**

- Visually lossless compression up to 4:1
- Even Mathematically Lossless capable at lower compression ratio
- Robustness to multiple encoding generations
- Fixed & Pixel lines-based latency
- Extremely light in FPGA (no external DDR memory)
- Fast in software
- Resolutions from HD to 4K/8K.

■

# ELSYS Eastern Europe: Semiconductor Design Center - Where Passion Leads to Excellence

Serbia-based ELSYS EE, which recently joined DSP Valley, provides a range of cost effective design services in microelectronics. The company attended the B2B Forum in Leuven where attendees could explore mutually beneficial cooperation projects.

## Semiconductor Design

ELSYS EE is a services company specializing in microelectronics. From its technical center in Belgrade, Serbia, ELSYS EE supports major international corporations, as well as mid-size highly specialized companies in their semiconductor design projects. ELSYS EE, composed of more than 100 highly skilled engineers, provides cost competitive design services, using the latest technology solutions.

## Expertise Overview

ELSYS EE has the ability to quickly staff and ramp up engineering teams for small to large projects in the area of digital, analog, mixed signal and RF integrated circuits. Work methods can be the ones of ELSYS EE (ISO 9001 & 14001 certified) or those of the customer.

ELSYS EE specialties include integrated circuit front end design, verification, physical implementation and embedded software development

## ELSYS EE know-how is divided in several domains:

**ASIC Front-End Design**

- Architecture, HDL RTL design
- Synthesis, DFT development
- Low power design
- Design of analog blocks
- Design flow automation

**ASIC Design Verification**

- eVC/UVC development
- eRM/UVM based env development
- Assertion based verification (SVA/PSL)
- Coverage driven verification, vPlan
- Automated post-silicon validation

**Analog Mixed-Signal Design, Verification and Physical Implementation**

- Physical layout design and verification
- Top-level/block-level AMS verification
- UVM based mixed-signal verification
- Analog modeling (Verilog/VHDL-AMS/ Verilog-A)
- Automated post-silicon validation

**FPGA Design**

- Architecture/RTL design/ Implementation
- Process-oriented design flow
- Testbench development & verification
- In-system validation, Device prototyping

**Embedded Software**

- Configuring and porting OS
- BSP and Device Driver development
- Bare-metal and Real-time development
- Functional and benchmark testing

## ELSYS EE is Member of a 1000 Engineer Group

ELSYS EE is part of the Advans Group, which gathers more than 1000 engineers in 7 countries. The Advans Group specializes in complex projects in the areas of electronic systems, applica-

ELSYS
EASTERN EUROPE

tion software and mechanics. In addition to its engineering services, the group develops technology solutions like embedded infotainment platforms or graphics IP, and spins-off/supports innovative start-ups.

### New DSP Valley Member

ELSYS EE has recently joined DSP Valley. According to Sasa Kostic, the Regional Director: *"We are glad to join this dynamic cluster, where entities can co-operate in a mutually beneficial way, and supports innovative start-ups/Spins-off.. We are looking forward to discussing with the group members in order to explore potential synergies."*

### Focus on Mixed-Signal Verification

Compared to what was common just a few years ago, analog and mixed-signal designs have become quite complex, particularly with the move to deep submicron CMOS. ELSYS EE can provide functional verification of complex analog and mixed-signal SoC designs. Its approach / methodology consists of modeling analog portions of the design using Verilog-AMS HDL and then integrating the models into UVM based verification environment. This concept ensures significantly faster simulations, thus obtaining UVM methodology to be fully applicable to the mixed-signal SoC designs. ■

# Flanders Make works with Flemish companies on self-driving vehicles

FLANDERS MAKE
MANUFACTURING INNOVATION NETWORK

Flanders Make, the strategic research center for the manufacturing industry, supports Flemish companies through the research program AVICA to develop technology for the realization of self-driving vehicles. With AVICA, Flanders Make focuses in first instance on self-driving buses for public transport. This way, the research center gives active support to both large and small Flemish companies to strengthen their long-term international competitiveness.

Flanders Make and the Flemish industry are working on the realization of self-driving buses that consider other road users and are able to participate in public road transport. This is a logical next step following the self-driving vehicles that are already in use, for instance in agriculture, in fields.
The research focus is on accurate positioning and the interpretation of the vehicle's environment and on establishing the right track that the vehicle should follow.

Dirk Torfs, General Director of Flanders Make, explains: *"With AVICA we are now focusing on self-driving buses for public transport as the whole value chain of companies for its successful realization is active in Flanders. Together with our partners, we realize a research platform for self-driving vehicles that will place Flemish technology in the international spotlights."*

Over the past 10 years, Flanders Make already acquired, together with Flemish companies and research organizations, comprehensive expertise in the field of, for instance, functional safety, vehicle systems that support drivers and track planning. The AVICA program builds on these foundations, with financial support from the Flemish government.

At this moment, the following organizations are already participating in projects that fit within the AVICA program: Dana, Induct, Siemens, Tenneco, TomTom, Transport & Mobility Leuven, University Gent, VDL Bus & Coach and Xenics Infrared Solutions. Flanders Make is open to interested companies to set up future research projects and continuously expands its network with organizations that want to help to realize this ambitious program. ■

# Imec and sureCore collaborate on SRAM Design IP

imec

sureCore Ltd., a low power SRAM IP company and imec announced a collaborating on low-power SRAM IP. The collaboration includes the licensing of a set of imec SRAM design IP to sureCore to expand sureCore's IP portfolio and a participation in sureCore. Moreover, sureCore will establish a branch in Leuven to tap into the design ecosystem around imec. The Leuven-based sureCore team will consist of highly experienced designers who built up their expertise at imec and who will be instrumental in the collaboration between sureCore and imec.

The collaboration will enable expertise of imec and sureCore to be pooled and shared to drive forward the development of low power SRAM IP solutions, e.g. for power issues of next generation wearable electronics and Internet of Things (IoT) applications, where extending battery life is crucial. It is also valuable in the networking space where power and heat dissipation are critical considerations. ■

# Implementing Real-Time Linux

ESSENSIUM
mind embedded development an ESSENSIUM division

## Abstract

Using Linux as a Real-Time Operating System (RTOS) might sound strange to someone familiar with the Linux kernel. In an RTOS, important tasks are guaranteed to be executed as soon as possible, at the expense of less important tasks. However, this is not how Linux has been designed.

The Linux kernel features a process scheduler named Completely Fair Scheduler (CFS), which as its name implies, tries to distribute time slices as fairly as possible over running processes. RT-Linux, short for Real-Time Linux, attempts to move away from such time-sharing approach and implements real-time behavior. A crucial part, discussed in this article, involves reducing latencies wherever possible, in order to ensure that critical jobs are run without much delay.

## Embedded Systems

If we take a look at typical embedded Linux applications we see a lot of examples that require the opposite behavior to real-time, namely optimized network throughput. To obtain better throughput you have to make sure that the task which is responsible for processing the network traffic gets enough time to get the job done. One approach to do that is to increase the scheduling latency and thus reducing the responsiveness of the system. Hence throughput and real-time are contradictory requirements.

## Implementations

There are 2 different approaches to implement real time in Linux. One approach is to combine Linux with an RTOS and a software layer that delegates all the real-time work to the real-time OS and the non-time-critical work to Linux. Sometimes the RTOS is implemented in hardware (for example in an FPGA). Another approach is to make changes directly in the existing kernel. For the rest of the article we will discuss this second approach, more specifically the Linux RT patches, or in short RT-Linux.

## Understanding Latency

In a real-time application the delay between some (hardware) event and its handling by the software, called latency, is an important factor. For a Linux system the latency can be defined as the sum of the following terms:

*kernel latency =*
*interrupt latency*
*+ interrupt handler duration*
*+ scheduler latency*
*+ scheduler duration.*

To guarantee that critical tasks are executed in time, a real-time OS will try to keep worst case kernel latency as low as possible. In practice a 'normal' (non-real-time) version of the Linux kernel will have a kernel latency in the order of milliseconds, RT-Linux in the order of microseconds. Let us have a look at the individual latencies and how RT-Linux tries to minimize them.

Interrupt latency is created because a new interrupt cannot be handled immediately, for example because a device driver might have temporarily disabled interrupts to prevent concurrent access, implemented by the spinlock_irq()-call. RT-Linux solves this by replacing the spinlock-calls by regular mutexes, this way concurrency is resolved by the mutexes and interrupts are not disabled.

Interrupt handler duration. In Linux interrupt handlers are split up into 2 parts. A top half that is executed as soon as the interrupt was triggered by the hardware, and a bottom-half that will be executed when all pending top-halves were finished. Top-halves have interrupts disabled. The execution time of the bottom half cannot be defined. If you need a real-time interrupt, use the top-half, bottom-half handlers cannot be used. RT-Linux solves this by using threaded-interrupt handlers. These handlers only check in their top-half if there is a bottom-half registered and all the 'handler-code' is moved to the bottom half. While this approach adds a little extra latency the interrupt handlers are now fully preempt-able and have their interrupts enabled hence reducing the interrupt latency. Also the threaded-interrupt handlers are controlled by software so it is possible to use priorities amongst interrupt handlers to further reduce latency in case there is extra load.

Scheduler Latency. This is the latency when switching from one process to the other. An important aspect is the preemption, the possibility of the OS to immediately schedule out a low priority process in favor of a higher priority task. Whether your kernel code is preempt-able or not depends on configuration, but when it is turned off the scheduler will keep running kernel code until an entire time slice was passed or another interrupt came in. This may leave the schedule of your real-time

task unbounded. RT-Linux solves this by making the entire kernel code preemptable.

Latency created by the scheduler and other non-deterministic factors.

The combination of virtual memory, on-demand data-load-and-execute and hardware caches leads to a great uncertainty in the execution-time of applications. Not to mention the fact that many standard libraries are not designed with real-time constraints in mind. There is no easy way to solve this besides quantifying this latency. Fortunately this latency is typically much smaller than the other ones.

## Conclusion

While the number of use cases where RT-Linux is a solution are limited and while active development on RT-Linux has recently stalled (although there seem to be a revival on using RT-Linux in drones !), experimenting with RT-Linux is a very interesting way to get a better understanding of the Linux OS and especially the process scheduler. This knowledge can be of use also in a non-real-time context: identifying and troubleshooting network-performance bottlenecks, device driver development, hardware CPU selection, etc.

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# Embedded Software Resilience

KU LEUVEN

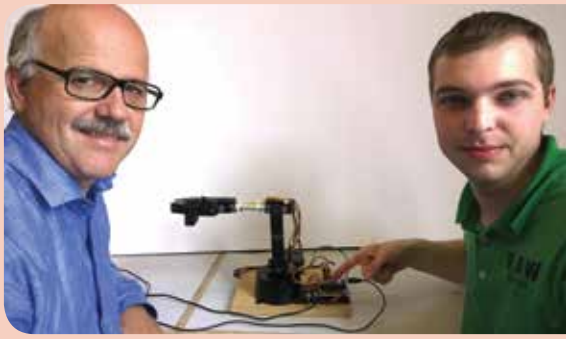
Embedded systems are being used more and more. This has led manufacturers of embedded systems to decrease the scale and supply voltage of their products. Combined with the harsh work environment, such as other electrical appliances and radiation, embedded systems are now prone to soft errors.

Soft errors are disturbances in hardware due to external factors. Soft errors lead to bit-flips in registers or other memory locations. The corrupted memory affects the software in execution, leading to data flow or control flow corruption. Data flow corruption results in wrong intermediary or output values. Control flow corruption affects the execution order of instructions. A control flow error leads to instructions being skipped or re-executed.

To minimize the effects of soft errors, they must be detected. Detection can be hardware- or software-based. While hardware-based detection, such as adding an extra shield to the PCB, may be more efficient than software-based detection, but it is also more expensive since it has to be installed on every produced device. Our research focuses on software implemented fault tolerance or SWIFT techniques. Examples of such techniques are defensive programming, signature monitoring and diverse programming.

To be able to compare the different detection techniques, some case studies will be implemented. One of the case studies is the robotic arm shown in the photo. Such a robotic arm is used in assembly lines. The arm is controlled by five servo motors which are driven by a pulse width modulated signal. A soft error can have different effects: it could shut down the PWM signal, it could move the robot to an unwanted position and many more.

The programs of the different case studies will each be protected with different SWIFT techniques. Each technique will be evaluated against predefined criteria, such as detection rate or run-time overhead. At the end of the experiments the results will be used to determine which technique is the best to detect soft errors in different situations. If no technique is the best, a decision tree will be constructed. This decision tree allows programmers to choose the technique that best meets their criteria.



***Left: Prof. dr. Ing. Jeroen Boydens, right: Ing. Jens Vankeirsbilck***

This research is in collaboration with Televic. To make it more suitable for their applications, the aspect of Functional Safety will be added to the research. One of the first tasks at hand is to determine if the soft error detection techniques can be implemented while complying with the rules of Functional Safety Standards.

## Research group

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# Trainings Mind

More info and locations available online
http://mind.be/training

## Android™ App Development Trainings

**September 16-18, 2015**
**Leuven, Belgium**

http://mind.be/training

This 3 days training is intended for developers who want to learn to write Android applications.
In a 50 to 60% lab-time approach, all participants get a real hands-on experience and they learn how to avoid classical Android pitfalls. The training first describes the Android architecture, and then covers all major parts of the API and application through theory and exercises. During the training, all attendees get direct feed-back in an interactive manner, and at the end of the training they are ready to work on their first real Android projects. ■

## Embedded Linux training

**September 21-25, 2015**
**Leuven, Belgium**

http://mind.be/training

This 5 days training is intended for developers who want to build an Embedded Linux system from scratch or from commercial Embedded Linux solutions.
The training covers the various components of an embedded Linux target, the development choices and the different debugging possibilities. A more detailed look is also taken at the Linux kernel architecture and important issues such as cross compilation and building of the main components. The training finishes with some more specific subjects to the choice of the participants (such as Real Time Linux, Qt development or building from distribution of choice). ■

## Linux Kernel and Device Driver Development Trainings

**September 28 - October 2, 2015**
**Leuven, Belgium**

http://mind.be/training

This 5 days training is intended for developers who want to learn how to write or improve Linux Kernel drivers for Embedded Linux platforms and Linux in general.
In a 50 to 60% lab-time approach, all participants get a real hands-on experience and they learn how to avoid classical pitfalls. The training goes deep into the kernel architecture, the main APIs, the integration of device drivers with other parts of the kernel and with user-space applications. During the training, all attendees get direct feed-back in an interactive manner, and at the end of the training they are ready to work on Linux device driver development projects. ■

## Nanotechnology for health 2015 presents visionary seminar and thematic sessions

**September 22-25, 2015**
**Imec, Leuven, Belgium**

www.imecacademy.be
http://bit.ly/Nanotechnologyforhealth

Imec academy and the doctoral schools of the 5 Flemish universities welcome you to the 3rd PhD-school on Nanotechnology for Health. Expert speakers will share the latest evolution in their field in tutorial style lectures.

The PHD-school starts with a visionary seminar, the 3 following days focus on thematic sessions. As a professional, you can subscribe to any of the course days. We are proud to announce internationally recognized keynote speakers and fascinating topics for the visionary lectures.

Jeff Wang (John Hopkins University), Håkan Jönsson (Royal Institute of Technology - SciLifeLab), Jeroen Lammertyn (KU Leuven), Wim Van Criekinge (Ghent University/MDxHealth), Sabeth Verpoorte (RU Groningen), Frank Speleman (Ghent University), Peter Peumans and Chris Van Hoof (imec) will provide you with the state of the art on:

- Customized chip technology for health
- All in one droplet: microfluidic chips for biomolecular assays
- Many droplets and single cells - droplet microfluidics in biomedicine and pharmaceuticals development
- Micro and nanobiosystems for diagnostics and life science research
- Translational epigenomics
- Organ-on-chip of particle manipulation and analysis on chip
- Body-area-networks and the future of healthcare
- The expanding universum of cancer epigenetics

The course continues for 3 more days covering the following fields more extensively:

- Epigenetics: mechanisms, tools, and applications
- Neuroscience: opportunities offered by nanotechnology, form imaging and modeling to treatments
- Lab-on-chip technologies: diagnostic sensors, devices, and platforms
- Single molecule techniques: microscopy and probing
- Body Area Newtorks (BAN): Communication Protocols, Circuits and Systems

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# SSIS October 20, 2015 Flanders - Belgium
## SMART SYSTEMS INDUSTRY SUMMIT

**October 20th, 2015**
**LAMOT Conference Center, Mechelen, Belgium**

http://www.ssis2015.com/

The Smart Systems Industry Summit (SSIS) is DSP Valley's international conference and exhibition on Smart Electronic Systems, organized right in the center of the vital DSP Valley eco-system.

The SSIS offers a unique networking and business platform. The summit brings together all major players, business and innovators in the field of micro and nano electronics. The attendance of captains of industry, experts, leading businesses, international representation, senior executives and government officials offers the possibility to engage in an interactive and innovative environment.

- Exclusive insights from executives, businesses and experts, representing the promising markets/ domains of nano and microelectronics
- Exposure to leading innovation in 'Designing Smart Products'
- Networking opportunities with potential partners, customers and investors
- Informal discussions during breaks and reception with executives, government officials, industry representatives and investors.

Parallel to the conference, a unique exhibition is held. The exhibitors showcase their latest functionalities, products and/or services as well as business tenders.

Welcome to Flanders high tech area!
Meet, feel and deploy the future together with DSP Valley and its members.

**Visit our website: www.ssis2015.com**

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continuation from page 15

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